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Applicant	:	T. WATANABE et al	
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Title	:	NEURAL NETWORK PROCESSING SYSTEM USING SEMICONDUCTOR MEMORIES	
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Examiner	:	J. Hirl	
Docket No.	:	HIT 2 482-06	
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APPEAL BRIEF

Sir:

This appeal is taken from the final rejection of claims 25-37 set forth in the Final Office Action dated February 11, 2005. In accordance with 37 CFR §41.37, the Appellant address the following items.

I. REAL PARTY IN INTEREST

The real party in interest of this application is Renesas Corp.

II. RELATED APPEALS AND INTERFERENCE

There are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 25-37 are currently pending. All of pending claims 25-37 have been finally rejected. Accordingly, the final rejection of claims 25-37 is being appealed.

IV. STATUS OF AMENDMENTS

No amendment has been filed after the Final Rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 25 is directed to a semiconductor integrated circuit device having a memory array, a processing circuit and an input/output circuit. The semiconductor integrated circuit device has a first mode and a second mode, wherein, in the first mode, a read operation and a write operation to the memory array are performed, and wherein the information stored in the memory array is read out to the input/output circuit in the read operation of the first mode and information outputted from the input/output circuit is written to the memory array in the write operation of the first mode (See Figs 11, 12 and 13(a) and Substitute Specification, page 30, lines 7-20; and page 31, line 30 to page 34, line 31). In the second mode, information stored in the memory array is read from the memory array to the processing circuit (See Figs 11 and 13(b) and Substitute Specification, page 30, lines 7-23; and page 34, line 32 to page 37, line 13). The processing circuit has an arithmetic unit and a MOS transistor which has a source/drain path between the

arithmetic unit and a power line and a gate inputted with a control signal. As shown in Fig 11, arithmetic unit 12 has a transistor T_3 that has a source/drain path coupled to power source VM. The gate of T_3 is fed arithmetic circuit starting signal ϕ_n (See Substitute Specification page 35, lines 14-30). During the first mode the MOS transistor is in an OFF state. In Fig. 13(a), it can be seen that the arithmetic circuit control signal NE is set so that ϕ_n is low during the first mode (memory mode) and therefore T3 is in an OFF state. The opposite is true in Fig. 13(b) (See Substitute Specification page 30 line 34 to page 31, line 1; and page 35, lines 9-10).

Independent claim 29 finds similar support as claim 25 and further defines a plurality of DRAM memory cells MC (See Fig. 11 and Substitute Specification page 29, lines 24-32). An input/output circuit IO includes latch circuits LAT (See Figs. 13(b), and 14(c) and Substitute Specification page 36, lines 15-20 and page 38, lines 28). As shown in Fig. 11, a first bus (pair of DA1) is coupled between memory array A and the logic circuit MT, a second bus NV is coupled between the logic circuit MT and the input/output circuit IO, and a third bus OA,IA is coupled between the first memory array and the input/output circuit IO. In a first mode, by using the third bus, information from outside the semiconductor chip is written to the first memory array or information stored in the first memory array is read out of the semiconductor chip from the first memory array (See Fig. 13(a) and corresponding description in Substitute Specification, particularly page 32, lines 23-26 and page 33, line 35 to page 34, line 6). In a second mode, by using the first bus, information is read from the first memory array to the logic circuit, by using the second bus, the

logic circuit outputs results of the operation to the latch circuit, and by using the third bus, data in accordance with the results is written to the first memory array (See Figs 13(b) and 14(c) and Substitute Specification page 34, line 32 to page 37, line 14; and page 38, lines 14-28).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 29-37 stand rejected under 35 U.S.C. §112, first paragraph as failing to comply with the enablement requirement. Claims 25-37 stand rejected under 35 U.S.C. §102(e) as being anticipated by Mashiko (U.S. Patent No. 4,988,891).

VII. ARGUMENT

1. Rejection under 35 U.S.C. §112

The Examiner's rejection of claims 29-37 under this section for failing to comply with the enablement requirement is apparently based upon the Examiner's attempt to read these claims only on Fig. 1 and its corresponding description in the specification. However, the subject matter of claims 29-37 mainly finds support in Figs. 11-14 (c) and their corresponding description.

(a) Independent Claim 29

It is submitted that this claim is adequately enabled and, as a result, so are its dependent claims. Appellant responds to each of the Examiner's points as follows.

With respect to item 5(a) of the Office Action, Appellant respond that the third bus corresponds to OA and IA as shown in Figs. 11, 13(a) and 13(b) . OA is a read line and IA is a write line (see Substitute Specification, page 32, lines 25-26 and page 36, lines 7-10). Therefore, it is submitted that the specification more than adequately describes that information from outside the semiconductor chip is written to a first memory array via a third bus. With respect to item 5(b), the first memory array and the second memory array correspond to arrays A and B shown in Fig. 11 (See Substitute Specification, page 29, lines 25-33). It is not necessary for the specification to specifically use the words "first" and "second". With respect to item 5(c) the first mode corresponds to the memory mode in Fig. 12 (See Substitute Specification, page 30, lines 17-20). It is not necessary for the specification to recite the word "first". Furthermore, the claims recite that a read operation and a write operation to the memory array are performed in the first mode. Finally, with respect to item 5(d) the latch circuit corresponds to LAT in Fig. 14(c) (See Substitute Specification, page 38, lines 25-28). In conclusion, if the claims are properly read in light of the specification, particularly the portions mentioned above, there should be no question as to whether the enablement requirement is satisfied.

(b) Dependent claim 30

This claim recites the second memory array which corresponds to array B, as mentioned above.

2. Rejection under 35 U.S.C. §102(e)

Claims 25-37 stand rejected under 35 U.S.C. §102(e) as being anticipated by Mashiko (U.S. Patent No. 4,988,891). This rejection is traversed as follows.

(a) Independent claim 25

Independent claim 25 is directed to a semiconductor integrated circuit device in which, in a first mode, a read operation and a write operation to a memory array are performed. The information stored in the memory array is read out to an input/output circuit in the read operation of the first mode and information outputted from the input/output circuit is written to the memory array in the write operation of the first mode. Furthermore, in a second mode, information stored in the memory array is read from the memory array to a processing circuit . The processing circuit has an arithmetic unit and a MOS transistor which has a source/drain path between the arithmetic unit and a power line and a gate inputted with a control signal. During the first mode the MOS transistor is in an OFF state. This allows for lower power consumption when the processing circuit is not carrying out operation.

Mashiko does not disclose or suggest two modes having features as in claim 25. Since the switching elements S1, S2, S3, S4 are each controlled by information stored in the random memory cells 150, 151, and output of an amplifier Ci, there is no disclosure of two modes as in claim 25. Also, Mashiko does not disclose or suggest a MOS transistor between an arithmetic unit and a power line, which is in a OFF state during a mode when read and write operations are performed.

The Examiner asserts that Mashiko discloses these feature of the claimed invention at column 3, lines 37-51 and column 6, lines 17-36. However, this portion of Mashiko merely discloses that random access memory cells 150 and 151 can be programmed from the exterior, but does not mention anything about reading out from RAM 150 and 151.

Independent claim 25 also recites that a MOS transistor of a processing circuit which has a source/drain path between the arithmetic unit and a power line and a gate inputted with a control signal is in an OFF state during the first mode. The Examiner attempt to rely upon Fig. 17 of Mashiko to disclose this feature is incorrect. Fig. 17 of Mashiko merely shows a driving circuit for a liquid crystal shutter array (see column 15, lines 42-53). Item 310 in Fig. 17 is a TN type liquid crystal cell and is not a processing circuit as recited in the pending claims (see column 15, lines 42-52). In view of this incorrect interpretation of Mashiko, it is submitted that the rejection of this claim should be reversed.

(b) Dependent claim 26

Dependent claim 26 further recites that the input/output circuit is for inputting and outputting data from and to outside of the semiconductor chip, and that a signal from outside the semiconductor integrated circuit controls whether the semiconductor circuit is in the first mode or the second mode. Since Mashiko is silent about the first and second mode, it follows that Mashiko is silent about any signal from outside the semiconductor integrated circuit that performs such control.

(c) Dependent claim 27

Dependent claim 27 further recites that there are a plurality of the memory arrays, that one of the plurality of memory arrays is selected in the first mode, and that the arithmetic unit is placed between two of the plurality of the memory arrays and receives outputs from the two of the plurality of memory arrays. Mashiko does not disclose the selecting of a memory array in the first mode and providing an arithmetic unit between two memory arrays to receive outputs from both, as claimed.

(d) Independent claim 29

The semiconductor integrated circuit device, as recited in claim 29, includes a first bus coupled between the first memory array and the logic circuit; a second bus coupled between the logic circuit and the input/output circuit; and a third bus coupled between the first memory array and the input/output circuit. The semiconductor integrated device also has a first and second mode. In the first mode, by using the third bus, information from outside the semiconductor chip is written to the first memory array or information is read out of the semiconductor chip from the first memory array. In the second mode, by using the first bus, information is read from the first memory array to the logic circuit. By using the second bus, the logic circuit outputs results of the operation to the latch circuit. Also, by using the third bus, data in accordance with the results is written to the first memory array.

Mashiko does not disclose or suggest a second bus coupled between the logic circuit and input/output circuit. While Mashiko does disclose a bus coupled between switching elements and random memory cells 150, 151, and a bus coupled between random memory cells 150, 151 and an interface (I/O), Mashiko does not disclose any separate bus for coupling the logic circuit and input/output circuit. Mashiko also does not disclose or suggest a first and second mode, as recited in claim 29. Clearly, since Mashiko does not disclose three separate buses as claimed, Mashiko cannot perform the memory function (first mode) and logic function (second mode) independently.

The following addresses some of the Examiner's comments and supports Appellant's position that the Examiner has misinterpreted the teaching of Mashiko. The Examiner states that the plurality of DRAM memory cells in claim 29 correspond to the RAM in Fig. 5 of Mashiko and that a third bus corresponds to programmed lines from the exterior. The Examiner further states that "programmed information re third bus will influence the output data that is written to the register . . . input/output". However, Mashiko discloses that the input/output data register is coupled to input lines and output lines, but does not disclose that programmed lines for the RAM are coupled to the input/output data register. Furthermore, the input lines and the output lines are not coupled to the RAM.

Therefore, Mashiko merely suggests in column 3, lines 52-58 how to select the RAM, but does not mention which lines are used to transfer programmed information to the RAM. Possibly, the programmed information is transferred to the

RAM of Mashiko via the bit lines in Fig. 5. As such, the programmed information is likely transferred from the bit decoder to the RAM, and not from the input/output data register to the RAM. Therefore, the programmed information for the RAM will not influence the output data that is written to the register.

The input lines and output lines correspond to lines A and B shown in Fig. 4 (see column 3, lines 7-8). In addition, the input lines A1 to A4 are respectively provided with amplifiers C1 to C4 which amplify the data on the corresponding input lines and transmit the same on to the corresponding output lines (see column 3, lines 24-27). Therefore, the input lines and the output lines are not coupled to the RAM. Instead, the RAM is merely coupled to word lines WL_1, WL_2 and BL. As such, it is submitted that all of the pending claims patentably define the present invention over Mashiko.

(e) Dependent claim 30

Dependent claim 30 further recites that a second memory array including a plurality of DRAM memory cells is provided such that the logic circuit is placed between the first memory array and the second memory array and receives outputs of the first memory array and the second memory array. Mashiko does not disclose such a structure. The Examiner argues that Fig. 1 of the specification does not disclose a second memory array. However, Fig. 11, for example, does disclose a second memory array and this limitation should be given patentable weight.

(f) Dependent claim 33

Dependent claim 33 further recites that the semiconductor integrated circuit device performs mode changing between the first mode and the second mode in accordance with a signal from outside of the semiconductor chip. Since Mashiko is silent about the first and second mode, it follows that Mashiko is silent about any signal from outside the semiconductor integrated circuit that performs mode changing.

(g) Dependent claim 34

Dependent claim 34 further recites that the logic circuit of semiconductor integrated circuit device includes an arithmetic unit and a MOS transistor which has a source/drain path between the arithmetic unit and a power line, and that during the first mode the MOS transistor is in off condition. Mashiko does not disclose the first and second modes and therefore does not disclose the status of the MOS transistor of the logic circuit during the first mode.

(h) Dependent claim 36

Dependent claim 36 further recites that a register is coupled between the first memory array and the logic circuit, and that in the second mode, the read operation and the write operation against the first memory array is performed concurrently. Mashiko is silent about any first or second mode and therefore do not disclose and concurrent reading and writing during that mode.

Conclusion

In conclusion, Appellant requests that the Board reverse all of the grounds of rejection by the Examiner. A Credit Card Payment Form is enclosed for the $500.00 filing fee for this Brief in support of an appeal.

If any further fees are due in connection with the filing of this Appeal Brief, including any Extension of Time fees that are necessary, the Commissioner is hereby authorized to charge Deposit Account No. 50-1417.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

25. A semiconductor integrated circuit device, comprising:

a memory array having a plurality of word lines, a plurality of bit lines, and a plurality of memory cells;

a processing circuit which carries out an operation using information stored in said memory array; and

an input/output circuit;

wherein said semiconductor integrated circuit device has a first mode and a second mode,

wherein, in said first mode, a read operation and a write operation to said memory array are performed,

wherein the information stored in said memory array is read out to said input/output circuit in said read operation of said first mode and information outputted from said input/output circuit is written to said memory array in said write operation of the first mode,

wherein, in said second mode, information stored in said memory array is read from said memory array to said processing circuit,

wherein said processing circuit has an arithmetic unit and a MOS transistor which has a source/drain path between said arithmetic unit and a power line and a gate inputted with a control signal, and

wherein during said first mode said MOS transistor is in an OFF state.

26. The semiconductor integrated circuit device according to claim 25, wherein said input/output circuit is for inputting and outputting data from and to outside of said semiconductor chip, and

wherein a signal from outside said semiconductor integrated circuit controls whether said semiconductor circuit is in said first mode or said second mode.

27. The semiconductor integrated circuit device according to claim 25, further comprising:

a plurality of said memory arrays,

wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and wherein said processing circuit is formed by MOS transistors,

wherein one of said plurality of memory arrays is selected in said first mode, and

wherein said arithmetic unit is placed between two of said plurality of said memory arrays and receives outputs from said two of said plurality of said memory arrays.

28. The semiconductor integrated circuit device according to claim 26, wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and said processing circuit is formed by MOS transistors, and wherein said semiconductor integrated circuit device is formed on a semiconductor chip.

29. A semiconductor integrated circuit device on a semiconductor chip, comprising:

a first memory array including a plurality of DRAM memory cells;

a logic circuit carrying out an operation using information stored in said first memory array;

an input/output circuit including latch circuits;

a first bus coupled between said first memory array and said logic circuit;

a second bus coupled between said logic circuit and said input/output circuit; and

a third bus coupled between said first memory array and said input/output circuit,

wherein said semiconductor integrated device has a first mode and a second mode,

wherein, in said first mode, by using said third bus, information from outside said semiconductor chip is written to said first memory array or information stored in said first memory array is read out of said semiconductor chip from said first memory array,

wherein, in said second mode, by using said first bus, information is read from said first memory array to said logic circuit, by using said second bus, said logic circuit outputs results of said operation to said latch circuit, and by using said third bus, data in accordance with said results is written to said first memory array.

30. The semiconductor integrated circuit device according to claim 29, further comprising:

a second memory array including a plurality of DRAM memory cells,

wherein said logic circuit is placed between said first memory array and said second memory array and receives outputs said first memory array and said second memory array.

31. The semiconductor integrated circuit device according to claim 29, further comprising:

a converting circuit which converts said results to said data so that a number of bits used for said data is equal to a number of bits used for information read out to said logic circuit,

wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor.

32. The semiconductor integrated circuit device according to claim 30, wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor.

33. The semiconductor integrated circuit device according to claim 30, wherein mode changing between said first mode and said second mode is performed in accordance with a signal from outside of said semiconductor chip.

34. The semiconductor integrated circuit device according to claim 29, wherein said logic circuit includes an arithmetic unit and a MOS transistor which has a source/drain path between said arithmetic unit and a power line, and wherein during said first mode said MOS transistor is in off condition.

35. The semiconductor integrated circuit device according to claim 29, further comprising:

a comparing circuit comparing said results with an expected value.

36. The semiconductor integrated circuit device according to claim 29, further comprising:

a register coupled between said first memory array and said logic circuit, wherein in said second mode read operation and write operation against said first memory array is performed concurrently.

37. The semiconductor integrated circuit device according to claim 29, wherein said first memory array and said second memory array each further includes sense amplifiers and a precharge circuit.

IX. EVIDENCE APPENDIX

There is no evidence relied upon in this appeal.

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.